those circuits is to be used is determined depending on whether the mode terminal IM3-0 is in a pull-up state or pull-down state. If the high-speed serial interfacing is selected, such an interfacing mode as shown in **FIG. 1** can be implemented. If the parallel interfacing is selected, such an interfacing mode as shown in **FIG. 6** can be implemented. Further, if low-speed serial interfacing is selected, it is possible to implement an interfacing mode where the low-speed serial interface is substituted for the parallel interface in the interfacing mode shown in **FIG. 6**. Thus, with the LCD drive and control device **10**, it is possible to ensure flexibility of a system configuration in respect of selectability of the interfacing mode with a host system.

[0079] The host module transmits a command and display data to the host interface circuit **20** by making use of a packet in a predetermined format. In the case of adopting the high-speed serial interface for the host interface, the command and the display data are received from differential data terminals Data ±. In the case of adopting the parallel interface for the host interface, the command and the display data are received from a data input/output terminal DBO-15. In the case of adopting the low-speed serial interface for the host interface, the command and the display data are received from a serial data input terminal SDI.

[0080] Upon receiving a command packet from the host module, the host interface circuit **20** stores address information as received through the packet in an index register (IDREG) **47**. The index register **47** decodes a command address as stored, and generates a register select signal, and so forth. Command data received through the packet is fed to a command data register array (CDREG) **46**. The command data register array **46** comprises a multitude of command data registers subjected to mapping at predetermined addresses, respectively. The command data register where the command as received is to be stored is selected by the register select signal outputted by the index register **47**. The command data latched by the command data register is fed to a corresponding part of the circuits, as an instruction or a control data, thereby controlling an internal operation. Further, it is also possible to directly select a command data register in the command data register array **46** to thereby set the command data in the command data register as selected.

[0081] Upon receiving a data packet from the host module, the host interface circuit **20** feeds address information of the data packet to an address counter (ACUNT) **49**. The address counter (ACUNT) **49** executes an incremental operation, and so forth, according to the content of the command data register corresponding to the address information to thereby execute addressing against a display memory (GRAM) **43**. If an access directive according to the command data at this point in time is to execute a write-operation against the display memory **43**, data of the data packet is fed to a write-data register (WDR) **42** via a bus **41** to be then stored in the display memory (GRAM) **43** at the same timing. Storage of the display data is executed, for example, on a display frame-by-display frame basis. If an access directive according to the command data is to execute a read-operation against the display memory **43**, data stored in the display memory **43** is read by a read-data register (RDR) **45** to be then rendered feedable to the host module. When the command data register receives the display data, the display memory **43** executes the read-operation in synchronization with display timing. A timing generator (TGNR) **50** executes timing control for reading and displaying. The display data read from the display memory **43**, in synchronization with the display timing, is latched by a latch circuit (LAT) **51**. The data as latched is given to a source driver (SOCDRV) **52**. The DISP **11** as a target for drive/control by the LCD drive and control device **10** is made up of a dot matrix TFT (thin-film transistor) liquid crystal panel, comprising drive terminals such as a multitude of source electrodes as signal electrodes, and a multitude of gate electrodes as scanning electrodes. The source driver (SOCDRV) **52** drives the source electrodes of the DISP **11** via a drive terminal S1-720. A drive level of the drive terminal S1-720 is controlled by use of a gradation voltage generated by a gradation voltage generation circuit (TWVG) **54**. The gradation voltage can be subjected to gamma correction by a gamma correction circuit (γ MD) **55**. A scan data generation circuit (SCNDG) **57** generates scanning data in synchronization with scanning timing given from the timing generator (TGNR) **50**. The scanning data is fed to a gate driver (GTDRV) **56**. The gate driver **56** drives the gate electrodes of the DISP **11** via a drive terminal G1-320. A drive level of the drive terminal G1-320 is controlled by use of a drive voltage generated by a liquid-crystal drive-level generation circuit (DRLG) **58**.

[0082] A clock pulse generator (CPG) **60** generates an internal clock by receiving source oscillation clocks from terminals OSC1, OSC2, respectively, to thereby feed the internal clock as an operation timing reference clock to the timing generator **50**. An internal reference voltage generation circuit (IVREFG) **61** generates a reference voltage to be fed to an internal logic power supply regulator (ILOGVG) **62**. The internal logic power supply regulator **62** generates an internal logic power supply on the basis of the reference voltage.

[Packet Control]

[0083] In **FIG. 1**, the MCU **5** transmits information to the LCD drive and control device **10** by making use of the packet in the predetermined format. The packet PKT includes a header part (HDR), and a body part (BDY), as shown in **FIG. 8** by way of example. The header part (HDR) has a packet data word-length region, an identification information region indicating the type of the packet, a parity code region, an address region FLDa, and so forth. The body part (BDY) has a data region FLDd.

[0084] The address region FLDa of the header part can include address information addrs, or specific code information splcd. The address information addrs means information on respective addresses assigned to address spaces inside the LCD drive and control device **10**, and the sub LCD drive and control device **12**, respectively. For example, in the case of the LCD drive and control device **10**, those addresses include the respective addresses of the command data registers of the command data register array **46**, register addresses of the index register **47**, respective addresses of the port registers **26** of the output port **22**, addresses of the register **36**, addresses of the display memory **43**, and so forth. In the case of the sub LCD drive and control device **12** as well, those addresses similarly include the respective addresses of the command data registers, the addresses of the display memory, and so forth. The specific code information splcd includes code information splcd **1** that can be assumed to specify the LCD drive and control device **10**, and